ABSTRACT

High speed memory access and transparent error detection and correction using a single error correcting means are obtained. A host computer writes sector data in one of the first memory and second memory, and next sector data in the other of the first and second memory. Sector data is read out from one of the first memory and second memory to the host computer, and simultaneously, next sector data is read out from the other of the first memory and second memory, and error detection and correction performed in the error correcting means. During a next cycle, the sector data read out from one of the first memory and second memory is outputted to the host computer, and simultaneously, error detection and error correction of the next sector data read out from one of the first computer and second computer is performed in the error correcting means.